# A Column-Parallel Inverter-Based Cyclic ADC for CMOS Image Sensor With Capacitance and Clock Scaling

Fang Tang, *Member, IEEE*, Bo Wang, *Student Member, IEEE*, Amine Bermak, *Fellow, IEEE*, Xichuan Zhou, *Member, IEEE*, Shengdong Hu, and Xiaoyong He, *Member, IEEE*

***Abstract*— This paper presents a low-power column-parallel inverter-based cyclic analog-to-digital converter (ADC) for CMOS image sensor readout circuit. By partially floating the capacitors inside the multiply digital-analog-converter during the least significant bit (LSB) quantization, the amplifier load capacitance could be significantly scaled down, which allows much higher settling speed and shorter cycle period. Since the signal-to-noise ratio for LSB cycle is relaxed due to the residual amplification, the proposed capacitance scaling only contributes ignorable input-referred quantization noise. Using the proposed techniques, a cyclic ADC can operate under 50% power consumption without suffering conversion rate, noise performance, and linearity. A 12-b quantization resolution test chip is fabricated using the TSMC 0.18-$\mu$m technology with 110 column-parallel ADC channels and 10.08-$\mu$m × 750-$\mu$m column pitch. The 3.5/−2 LSBs integral nonlinearity and 10.1-b effective-number-of-bit are measured under 2-$\mu$s sampling rate with 120-$\mu$W power consumption per channel.**

***Index Terms*— CMOS image sensor, column-parallel circuit, cyclic analog-to-digital converter (ADC), low power, mixed signal.**

## I. Introduction

CYCLIC analog-to-digital converter (ADC) is widely used in moderate-resolution moderate-speed data conversion applications [1]. It gets benefit from simple structure when compared with a pipelined ADC and smaller scale capacitor array design against successive-approximation ADC. Several techniques were introduced in the prior arts to make better tradeoff between conversion speed, power consumption, and design complexity, such as well-known 1.5-b-per-stage error correction [2] and capacitor sharing [3]. Besides of those common techniques, incompletely settled sampling was proposed in [4] and [5]. The basic idea behind is that the voltage settling for least significant bit (LSB) has lower requirements compared with most significant bit (MSB) quantization, from the perspective of input-referred error. Therefore, the conversion time in each cycle is able to be elaborately controlled and as a result, the LSB quantization speed can be enhanced. Besides the timing optimization, efforts were made also in amplifier optimization. One of the attractive trends in multiply digital-to-analog converter (MDAC) amplifier innovation is replacing the traditional operational transconductance amplifier by an inverter amplifier. This inverter-based integrator had been widely analyzed for sigma-delta ADC implementation [6]–[8]. Most of the inverter-based amplifiers are still using single-stage structure with different gain-boosted methods. True three-stage inverter amplifier or ring amplifier was proposed in recent years. According to the traditional knowledge, closed-loop three-stage inverter could lead to oscillation. A well designed bias condition was implemented by splitting the second-stage inverter into two identical ac-coupled paths to prevent oscillation [9]. A self-biased three-stage ring amplifier for switched-capacitor circuit was presented in [10]. To improve the practicality of ring amplifier, low noise was optimized in the first inverter stage, switches were eliminated and a resistor was adopted in second stage for self biasing.

In this paper, we report a power-optimized inverter-based cyclic ADC scheme. By partially floating the sampling capacitor and also the feedback capacitor inside the MDAC, the main amplifier during the LSB conversion enjoys significant load reduction. As a result, the LSB cycles can operate much faster than the MSB cycles. The proposed capacitor scaling technique only introduces ignorable extra quantization noise due to residual voltage amplification, which is silicon proved in 0.18-$\mu$m CMOS process in this paper.

This paper is organized as follows. In Section II, the typical column-parallel cyclic ADC for CMOS imager is introduced. Section III presents the proposed power optimized cyclic ADC scheme. Section IV describes the circuit implementation of the proposed design. Section V demonstrates the measurement results.

## II. Column-Parallel Cyclic ADC

Also known as algorithmic converter, cyclic converter is one of the serial ADC schemes and requires $N$ cycles to

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F. Tang, X. Zhou, and S. Hu are with the College of Communication Engineering, Chongqing University, Chongqing 400044, China (e-mail: frankfangtang@gmail.com; zxc@cqu.edu.cn; husd@cqu.edu.cn).

B. Wang and A. Bermak are with the Department of Electronics and Communication Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: timepicker@gmail.com; eebermak@ust.hk).

X. He is with the South China University of Technology, Guangzhou 510641, China (e-mail: eemorrishe@scut.edu.cn).

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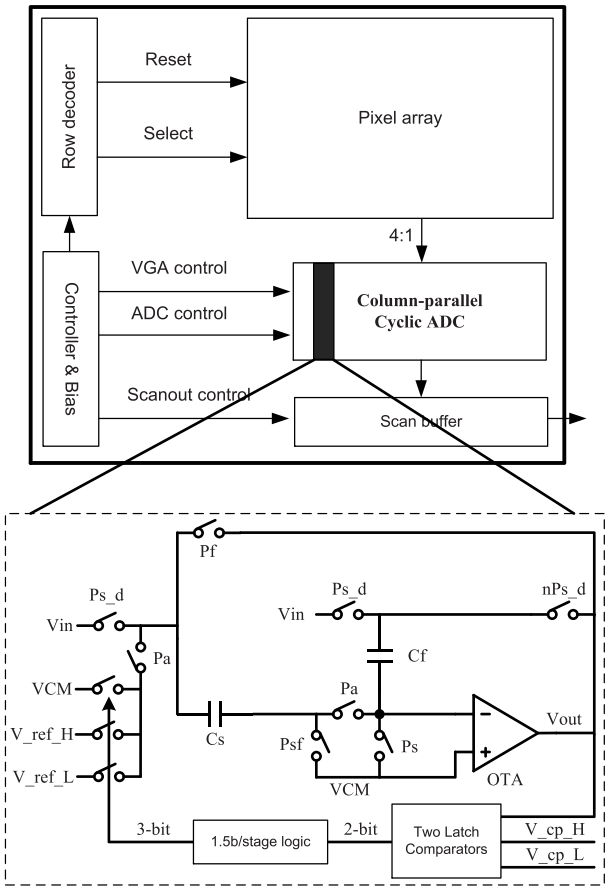


Fig. 1. Schematic of a typical single-ended cyclic ADC with capacitor sharing topology.

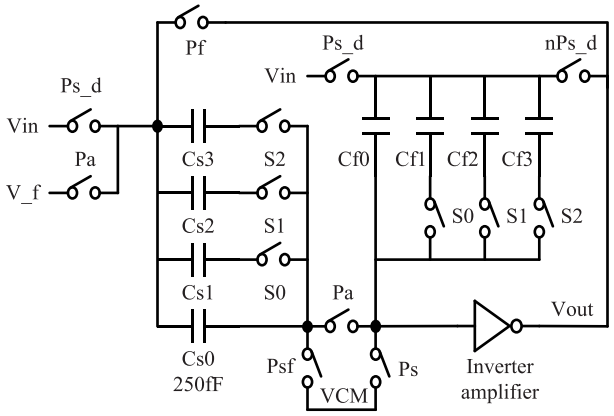


Fig. 2. Schematic of the proposed MDAC of a cyclic ADC.

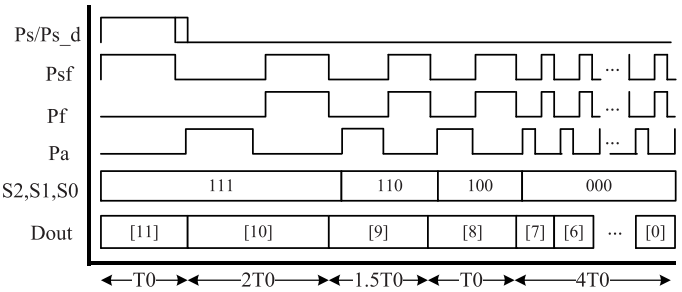


Fig. 3. Timing diagram of the proposed cyclic ADC.

complete a $N$-bit conversion, which is similar to successive approximation ADC. Fig. 1 shows a typical cyclic ADC schematic with capacitor sharing topology used for CMOS image sensor column-parallel readout circuit. The MDAC can be configured with 1.5-b-per-stage topology, which consists of a main amplifier, two capacitors $C_s$ and $C_f$, multiphase-controlled switch transistors, two latch comparators and digital logics. V_cp_H and V_cp_L are the two latch comparator reference voltages used to generate the control input of the 1.5-b-per-stage logic circuit. V_ref_H, V_ref_L, and common-mode voltage (VCM) are the digital-to-analog feedback voltages, which are determined by the 3-b results from the logic circuit [3]. The capacitor $C_f$ is used in both sampling phase and charge transferring phase. By such a capacitor sharing technique, $C_s$ and $C_f$ only need identical capacitance to be able to achieve $\times 2$ residual voltage amplification.

Cyclic ADC has the similar MDAC topology as a pipelined ADC. But by reusing the MDAC in each quantization cycle, only one stage MDAC is necessary. In pipelined ADC, each MDAC stage enjoys a scaled input-referred noise, which is attenuated by its front-end gain. However, the cyclic ADC is difficult to optimize in each cycle due to a fixed single stage MDAC topology. For example, $C_s$ and $C_f$ have a constant capacitance for each bit quantization. Therefore, the amplifier must always drive a large capacitance load even during the LSB conversion. The traditional features of unscaled capacitance and fixed cycle period in cyclic ADC leaves a considerable headroom for low-power optimization.

## III. Proposed Design

The circuit schematic of the proposed cyclic ADC MDAC is shown in Fig. 2 and the timing diagram is shown in Fig. 3. Sampling capacitor ($C_s$) and the feedback capacitor ($C_f$) are divided into four subcaps with a unit capacitance of 250 fF for each subcap. Subcap 1 $C_{s0}$ and $C_{f0}$ are hard connected, while the other three are transfer-gate-controlled by S0∼S2. During the sampling phase ($P_s$), all capacitors are connected to the input, which has a total input capacitance of 2 pF. In quantization phase, the feedback capacitor ($C_f$) is connected to the amplifier output $V_{\text{out}}$ controlled by the inverted delayed-sampling logic nPs_d. During the first two conversion cycles, S0∼S2 keep closed and the capacitor-shared 1.5-b-per-stage ADC operates under a fixed clock period ($T_0$). When entering in the third conversion cycle, S0 is open, while S1 and S2 remain closed thus, both $C_s$ and $C_f$ have only 3/4 total capacitance. Since the amplifier load is reduced, we can accordingly shrink the cycle period to 3/4. Similarly, the fourth and fifth cycles also enjoy speed enhancement by sequentially disconnecting S1 and S2. Finally, both $C_s$ and $C_f$ have only 1/4 total capacitance and the operation frequency of the ADC is boosted up to four times from the sixth cycle until the beginning of the next input sampling. Assuming the input sampling consumes a period of $T_0$ and the first quantization cycle period is $2T_0$, the proposed cyclic ADC requires

only $9.5T_0$ conversion time. In a conventional cyclic ADC design, without using the proposed capacitance and clock scaling techniques, if bit 0∼10 have the same quantization period of $2T_0$, the total conversion period could be more than $23T_0$

$$\overline{n_{\rm ir}{}^2} = \sum_{i=0}^{11} \frac{\overline{n_i{}^2}}{W^{\rm i}} = \sum_{i=0}^{11} \frac{\overline{n_i{}^2}}{4^{\rm i}}. \tag{1}$$

The input-referred random noise power ($\overline{n_{\rm ir}{}^2}$) of a 12-b cyclic ADC can be expressed as (1). Where $W_i$ is the input-referred noise weight in conversion cycle $i$. For 1.5-b-per-stage scheme, the noise power weight is approximately equal to $1/(4^i)$. $\overline{n_i^2}$ is the random noise power in conversion cycle $i$, which consists of KT/C and the amplifier noise. The designed amplifier noise is relatively much smaller than KT/C noise, since amplifier circuit is a fixed design but capacitor faces scaling down during quantization. Here, the amplifier noise is ignored to simplify the analysis. Thus, the conventional cyclic ADC has a input-referred noise power about $\overline{n_{\rm irc}{}^2}$ which equals to $1.33\alpha\overline{n_i^2}$ assuming noise power for each cycle keeps constant. It is clear that, compared with the MSB conversion cycle, the LSB cycle contributes much less input-referred noise due to the residue amplification. With the proposed capacitor scaling technique, the $\overline{n_i^2}$ is cycle-dependent, which can be expressed as (2). The input-referred noise power of the proposed scheme could be derived as (3), which is increased from 1.33 to 1.39, indicating no more than 5% noise power or 3% voltage noise increase. It should be noted that, to achieve the same noise specification, the total capacitance of the proposed scheme need to increase ∼10% to compensate the scaled-down capacitor. According to the simulation result under identical noise requirement, the proposed technique still enjoys more than 40% energy efficiency enhancement when compared with the conventional ADC scheme

$$\begin{aligned} \overline{n_i{}^2} &= \alpha \frac{\rm KT}{C_i} \\ C_i &= \{C_{\rm Tot}, 3/4C_{\rm Tot}, 1/2C_{\rm Tot}, 1/4C_{\rm Tot}\} \end{aligned} \tag{2}$$

$$\overline{n_{\rm ir}{}^2} = \sum_{i=0}^{11} \frac{\alpha \frac{\rm KT}{C_i}}{4^{\rm i}} = 1.39\alpha \frac{\rm KT}{C_{\rm Tot}}. \tag{3}$$

## IV. Chip Implementation

An unconditionally stable gain-boosted inverter amplifier with offset autozeroing switch is adopted in this paper, as shown in Fig. 4. Because the pixel is operated under 3.3 V supply in 0.18-$\mu$m CIS process, the inverter amplifier also uses 3.3 V transistors to cover the high-voltage region and meanwhile providing a large dc open-loop gain of more than 68 dB. The gain-boosted inverter amplifier loses the low-voltage region, since the output swing is limited by the regulator nMOS transistor M4. In order to compensate the lost output swing, M1∼M4 are deep-n-well nMOS (DNMOS) transistors. The body of the DNMOS is connected to a negative voltage of −0.9 V, which is generated by an on-chip charge pump. All DNMOS transistors in each ADC channel operate under the same negative supply, the deep n-well from each channel

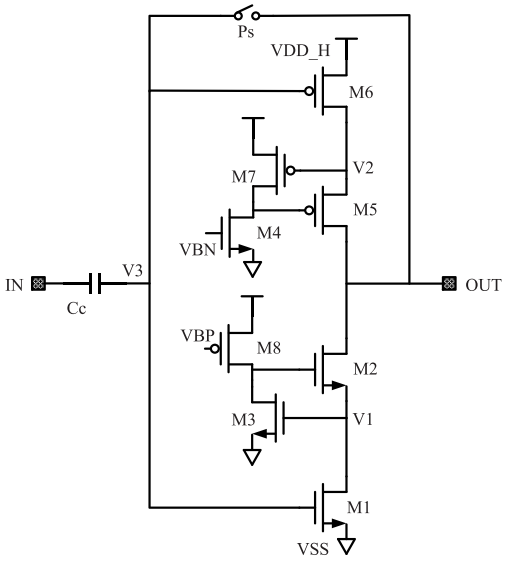


Fig. 4. Schematic of the gain-boosted inverter amplifier.

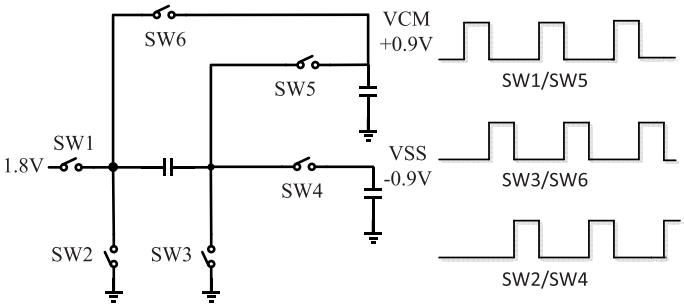


Fig. 5. Schematic of the single flying capacitor charge pump and the operating timing diagram.

can be tied together as a large single plane deep n-well. Therefore, the chip area increase is affordable. During the autozero phase, $V3$ is reset to 1.2 V and during charge transferring phase, $V3$ is kept near this voltage due to a large open-loop gain. $V1$ and $V2$ are clapped ∼2.6 and −0.2 V, respectively, using the gain boosted circuit. According to the simulation result, the highest gate-to-diffusion voltage of all transistors is no more than 3.3 V even with 3.3/−0.9 V power supply on the inverter amplifier. If the column-parallel quantization circuit is turned OFF, the negative supply should short to 0 V inside the charge pump, in order to prevent the unsafe gate-to-diffusion voltage. Therefore, there is no potential gate break-down risk. Moreover, $V1$, $V2$, and $V3$ voltages have weak input-signal dependence in theory, due to the high dc gain and auxiliary amplifier. As a result, the current flowing through transistor M1 to VSS can be considered stable.

The charge pump in this paper adopts a single flying capacitor scheme, as shown in Fig. 5 [13]. The SW1∼SW6 operate under half charge pump mode controlled by the three-phase clock and ±0.9 V are pumped into the two output load capacitors, respectively. The 0.9 V output is designed for the dedicated common-mode voltage VCM, while the −0.9 V output is used for the negative power supply VSS in the inverter amplifier. The charge pump efficiency is determined by the operating frequency, flying capacitance,

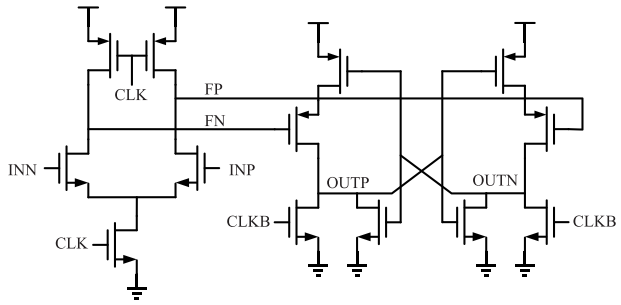


Fig. 6. Schematic of the low kickback noise latch comparator.

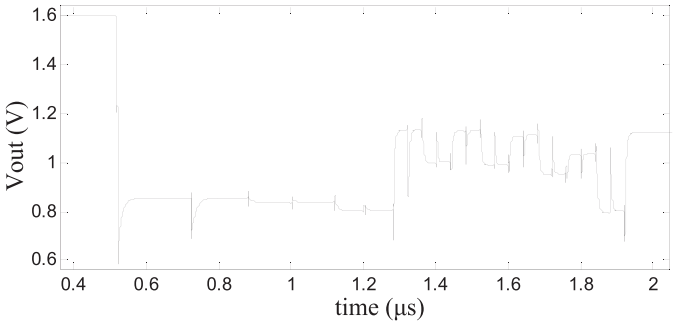


Fig. 7. Simulation result of the charge transferring output of the MDAC in TT corner under room temperature.

and switch turn-ON resistance. Higher capacitance and lower resistance are useful to achieve a more smooth and noiseless output voltage, however, with extra cost of chip area. In this paper, the on-chip capacitor is ∼1 nF with extra 1 $\mu$F external discrete capacitor on the output load. The switch is sized for 0.2 Ω turn-ON resistance. For a large ADC array or a high image frame rate, fast clock frequency of the charge pump or huge on-chip decap cannot efficiently guarantee the voltage stability because the settling voltage of the charge pump is obviously affected by the large load current. On such a condition, alternative solution is preferred such as using external negative power supply, on-chip dc–dc converter or low-drop-out regulator to stabilize the supply voltage.

The latch comparator in this paper is shown in Fig. 6. Because the second latch stage is isolated from the input node and both FN and FP have the similar decreasing behavior during evaluation phase, the kickback noise in the input node can be significantly reduced. All circuits operate in fully dynamic mode and no static current is consumed. Fig. 7 shows the simulation result of the charge transferring output of the entire MDAC during a complete analog-to-digital conversion. Due to the scaled load capacitance, the main amplifier output voltage can be fully settled with scaled slew rate during the whole conversion cycles.

## V. Measurement Results

Fig. 8 shows the chip microphotograph of the proposed readout circuit fabricated using TSMC 0.18-$\mu$m CMOS technology. The charge pump is located in the corner of the core circuit with nanofarad on-chip decap load.

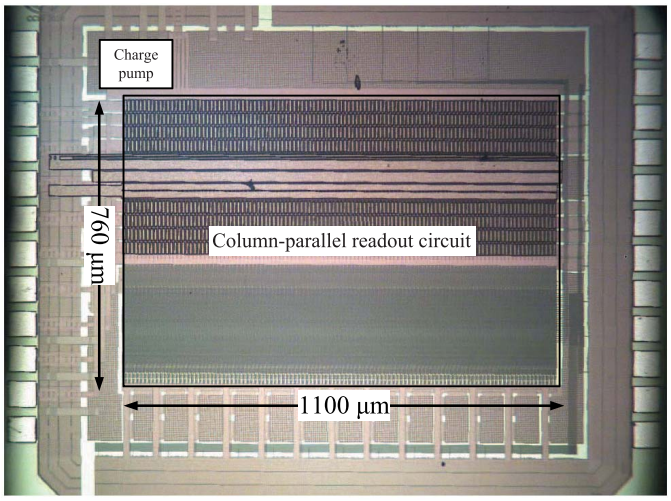


Fig. 8. Microphotograph of the proposed readout circuit.

TABLE I
Performance Summary of the Proposed ADC

| Specification | Measurement result | |
|---|---|---|
| | Proposed scaling mode | Conventional Non-scaling mode |
| Resolution | 12-bit | 12-bit |
| SINAD | 62.68 dB | 63.0dB |
| SNR | 64.82 dB | 65.5dB |
| THD | -66.79 dB | -66.6dB |
| SFDR | 68.23 dB | 68.1dB |
| SNDR | 62.68 dB | 63.0dB |
| ENOB | 10.1-bit | 10.2-bit |

The 10-$\mu$m p+ type guard ring and 10-$\mu$m n-well type guard ring are added around the charge pump to isolate the large clock noise. The core area of the column-parallel circuit is ∼1100 $\mu$m × 760 $\mu$m. The 110 ADC channels are implemented with 10.08-$\mu$m column pitch in order to fit two column digital standard cells in each ADC channel. Therefore, the implemented column-parallel readout circuit can be used for 5.04-$\mu$m pixel pitch when placing a readout circuit bank in both sides of the pixel array [12]. The power consumption of each 12-b ADC channel is ∼120 $\mu$W under 2-$\mu$s sampling rate, which means 210 ns $T_0$.

Fig. 9 shows the differential nonlinearity (DNL) and the integral nonlinearity (INL) of the proposed ADC, which verifies no missing code and less than 3.5/−2 LSBs INL distortion. The input voltage is from zero to 1.8 V. To verify the dynamic performance of the proposed ADC, a 10 K points fast Fourier transform (FFT) with 51-kHz sinusoid input signal is measured under 500-kHz sampling rate, as shown in Fig. 10(a). The 10.1-b effective-number-of-bit (ENOB) is silicon proved, while the total harmonic distortion is about −66.8 dB. The distortion free signal-to-noise ratio is ∼64.8 dB. The performance of the proposed ADC is summarized in Table I,

TABLE II
SUMMARIZED COMPARISON WITH PRIOR ARTS OF COLUMN-PARALLEL ARCHITECTURES

| Column-parallel Architecture | Folding-Integration/Cyclic [1] | Folding-Integration/ Cyclic [3] | Two-Stage Cyclic [14] | SAR [15] | Single Slope /SAR [12] | SAR/SS [16] | This work |
|---|---|---|---|---|---|---|---|
| Year | 2012 | 2012 | 2012 | 2012 | 2013 | 2014 | - |
| ADC resolution | 13-19 bits | 17-bit | 12-bit | 10-bit | 11-bit | 9-bit | 12-bit |
| Main design requirement | Traditional OTA performance | Traditional OTA performance | OTA Two stages | Digital calibration | 3-bit SSADC +8-bit SAR | 6-bit SAR +3-bit SSADC | +/- 0.9V supply, Scaling scheme |
| Technology | 0.18μm 1P4M CIS | 0.18μm 1P4M CIS | 0.18μm 1P4M CIS | 0.18μm | 0.18μmCIS | 0.18μm | 0.18μm |
| DNL | <+0.4/-0.6 % | +1.3/−0.8LSB | +0.63/-0.55LSB | 0.55LSB | +1.65/-1.45LSB | 9.9 LSBs | <+/-0.5 LSBs |
| INL | +/-4LSB @ 17-bit | +35/−25LSB @ 17-bit | +3.7LSB /-0.8LSB | 0.77LSB | - | +4.7 /-9.8 LSBs | +3.2/-2 LSBs |
| SNDR or ENOB | - | - | - | 9.83-bit | - | 6.3bit | 62.68 dB/10.1bit |
| Power consu. | 450mW @10MHz clock | 132 μW/channel @ 30fps 1352row | 101μW/ channel @120fps 7680row | 58 μW/channel @ 768 KSamp | 1.33 mW /Mpixels.frame | - | 120 μW/ channel @2 μs period |
| FOM=power /conversion state | - | 3.25 nJ/pixel | 109 pJ/pixel | 74 fJ/state | 1.33 nJ/pixel | 12 pJ/pixel | 241.6 fJ/state 240 pJ/pixel |

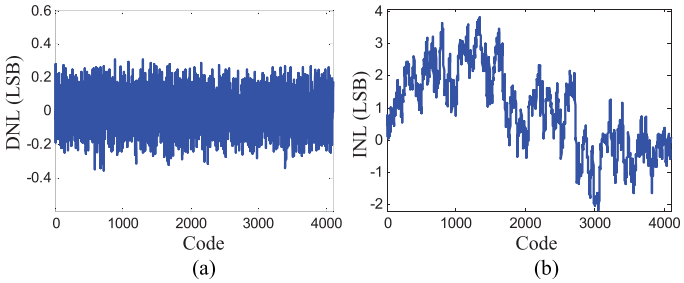


Fig. 9. Measurement result of (a) INL and (b) DNL.

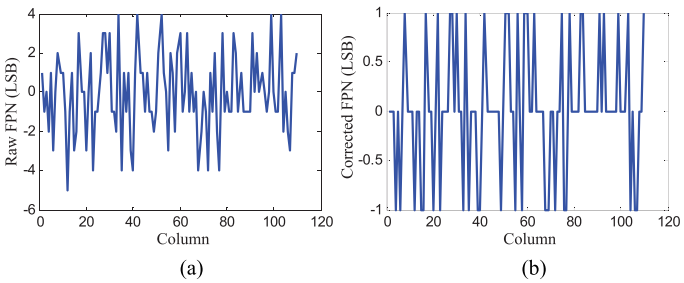


Fig. 11. Measurement result of the FPN (a) without and (b) with digital CDS.

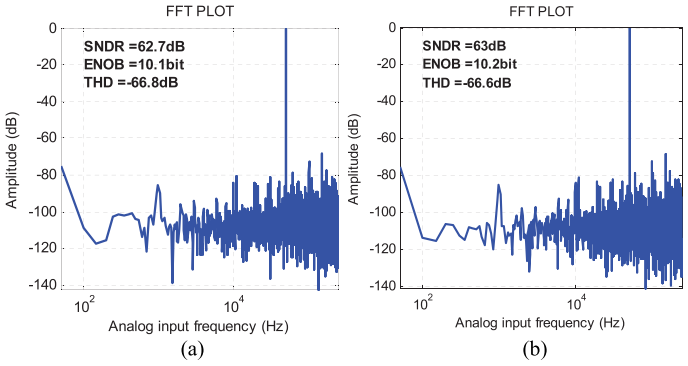


Fig. 10. Measurement result of the power spectrum density in the proposed (a) capacitance and clock-scaling mode and (b) conventional nonscaling mode.

compared with the ADC measurement results operating under conventional nonscaling mode. A slight 0.1-b ENOB increase under the conventional mode is observed according to the same condition FFT analysis, as shown in Fig. 10(b), where the results are within the trend expectation indicated from (3). Data from the 50th ADC channel is used for the spectrum measurement. The intercolumn offset mismatch or fixed pattern noise (FPN) is measured as shown in Fig. 11. The 4/−5 LSBs raw FPN is observed, showing about 10-b columnwise offset consistence. By applying digital correlated-double-sampling (CDS), the corrected FPN is reduced to only ±1 LSB. The system-level specification comparison against to the prior arts in recent years are summarized in Table II.

## VI. CONCLUSION

In this paper, a novel low-power cyclic ADC scheme is presented. Using capacitor and clock scaling technique, the cyclic ADC can operate 2 times and 4 times faster in fourth quantization cycle and after fifth cycle, respectively. As a result, the proposed ADC enjoys more than 50% higher energy efficiency with only 3% voltage quantization noise increase or it achieves 40% higher energy efficiency while keeping the same noise performance. The proposed circuit is fabricated using 0.18-$\mu$m CMOS process, showing the completed charge transferring settlement for a 12-b cyclic ADC without missing code and less than 3.5/−2 LSBs INL. The raw columnwise FPN is 4/−5 LSBs and after digital CDS, the FPN is corrected to ±1 LSB. The proposed cyclic ADC could be an attractive solution for the next generation low-power high-pixel resolution CMOS image sensor column-parallel readout circuit.

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**Fang Tang** (S'07–M'14) received the B.S. degree from Beijing Jiaotong University, Beijing, China, in 2006, and the M.Phil. and Ph.D. degrees from The Hong Kong University of Science and Technology, Hong Kong, in 2009 and 2013, respectively.

He was a Research Associate with The Hong Kong University of Science and Technology. He has been a Distinguished Research Fellow and Tenure-Track Assistant Professor with Chongqing University, Chongqing, China, since 2013.

**Bo Wang** (S'13) received the B.Sc. degree from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2010, and the M.Phil. degree from the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2012, where he is currently pursuing the Ph.D. degree with the Department of Electronic and Computer Engineering.

**Amine Bermak** (M'99–SM'04–F'12) received the M.Eng. and Ph.D. degrees in electronic engineering from Paul Sabatier University, Toulouse, France, in 1994 and 1998, respectively.

He is currently a Full Professor and an Associate Head with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, where he is also the Founder and the Leader of the Smart Sensory Integrated Systems Research Laboratory.

**Xichuan Zhou** (S'06–M'13) received the B.S. and Ph.D. degrees from Zhejiang University, Hangzhou, China, in 2005 and 2010, respectively.

He has been an Associate Professor and the Assistant Dean with the College of Communication Engineering, Chongqing University, Chongqing, China, since 2010. He has authored over ten articles in journals and conference proceedings. His current research interests include large-scale system design, optimization, and application.

**Shengdong Hu** received the Ph.D. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2010.

He is currently an Associate Professor with the College of Communication Engineering, Chongqing University, Chongqing, China. He has authored over ten journals. His current research interests include power electronics and semiconductor devices.

**Xiaoyong He** (M'10) received the bachelor's degree in microelectronics technology and the master's degree in solid-state electronics from the Huazhong University of Science and Technology, Wuhan, China, in 1997 and 2000, respectively, and the Ph.D. degree in electronic engineering from The Chinese University of Hong Kong, Hong Kong, in 2010.

He joined the South China University of Technology, Guangzhou, China, in 2012, as an Associate Professor.